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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,931	03/04/2002	Donald R. DeSota	BEA920010023	3811

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EXAMINER	
DUNCAN, MARC M	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,931	DESOTA ET AL.	
	Examiner	Art Unit	
	Marc M Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-20* is/are rejected.

7)☒ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claims 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-4, 8-9 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kane et al.

Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kane and ESC as applied to claim 10 above, and further in view of Zhang.

Claims 10, 11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kane in view of ESC Technologies.

Claims 5-7 are objected to.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The means in the medium, as recited in claim 18, are not computer executable and the means are not executing. There is no functional interrelationship between the computer and the means in the medium. The claim is therefore non-statutory.

Claim 20 recites a modulated carrier signal. A modulated carrier signal does not fall into any of the four statutory classes. A modulated carrier signal is neither concrete nor tangibly embodied. The claim is therefore non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 8-9 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kane et al.

Regarding claim 1:

Kane teaches retrieving a cache entry for a desired memory address, the cache entry including data and a stored error-correcting code (ECC) based at least on the data and a memory address in Fig. 5 and paragraphs 0056-0058.

Kane teaches determining an ECC based on at least the data of the cache entry and the desired memory address in Fig. 6A and paragraph 0060. The new ECC is calculated based on the data at a cache location that matched the desired address and is therefore determined based on the data of the cache entry and the desired memory address.

Kane teaches upon determining that the ECC based at least on the data of the cache entry and the desired memory address equals the stored ECC, concluding that the cache entry caches the desired memory address without error in Fig. 6A and paragraphs 0061-0062.

Regarding claim 2:

Kane teaches otherwise, retrieving a primary memory entry for the desired memory address in paragraph 0064. When a cache miss is declared, the data is necessarily retrieved from the primary memory. This is an inherent function of a cache.

Regarding claim 3:

Kane teaches determining whether the cache entry caches the desired memory address with error in Fig. 6A and paragraphs 0061 and 0063. The ECC value is checked to determine whether the cache entry caches the memory address with an error and, if so, an attempt is made to correct the error.

Regarding claim 4:

Kane teaches determining whether the cache entry caches a memory address other than the desired memory address in Fig. 6A and paragraphs 0062. If a parity error has occurred in the cache, the address is an address other than the desired address.

Regarding claim 8:

Kane teaches wherein determining the ECC comprises determining the ECC based on the data of the cache entry and a tag of the desired memory address in Fig. 4, Fig. 5 and paragraphs 0054 and 0056-0058. Kane teaches the use of address tags for accessing a cache.

Regarding claim 9:

Kane teaches wherein determining the ECC based on at least the data of the cache entry and the desired memory address comprises determining the ECC also

based on a state of the cache as to the cache entry in paragraph 0043 and Table 1. Mtags are embedded in the data. Mtags represent the state of the cache as to the cache entry.

Regarding claim 18:

The claim is rejected as the computer readable medium containing computer readable instructions that, when executed, perform the method of claim 1.

Regarding claim 19:

The claim is rejected as the computer readable medium containing computer readable instructions that, when executed, perform the method of claim 9.

Regarding claim 20:

Kane teaches wherein the medium is one of a recordable data storage medium and a modulated carrier signal in paragraph 0073.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 10, 11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kane in view of ESC Technologies.

Regarding claim 10:

See the teachings of Kane above.

Kane further teaches a primary memory having a number of memory entries corresponding to a plurality of memory addresses in paragraph 0002.

Kane does not explicitly teach the primary memory having a primary ECC based on the stored data. Kane does, however, teach a system that must meet performance and reliability standards.

ESC teaches a primary memory having a primary ECC based on the stored data in the definition of ECC memory.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the ECC memory of ESC with the system of Kane.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Kane states an explicit need for a system to meet performance and reliability expectations. The ECC memory of ESC meets that need by providing a memory that is fault tolerant and reliable.

Regarding claim 11:

Kane teaches wherein the cache comprises a one-way cache, such that each memory entry of the primary memory can be cached in only one of the number of cache entries in the entire document. The cache described by Kane is a one-way cache.

Regarding claim 13:

Kane teaches wherein the controller, for each desired memory address, retrieves the memory entry for the desired memory address from the primary memory upon concluding that the ECC determined for the desired memory address does not equal the stored ECC for the cache entry for the desired memory address in paragraph 0064. When a cache miss is declared, the data is necessarily retrieved from the primary memory. This is an inherent function of a cache.

Regarding claim 14:

Kane teaches wherein each of the stored ECC and the ECC determined is based on at least the data and a tag of the memory address in Fig. 4, Fig. 5 and paragraphs 0054 and 0056-0058. Kane teaches the use of address tags for accessing a cache.

Regarding claim 15:

Kane teaches wherein each of the stored ECC and the ECC determined is also based on a cache state in paragraph 0043 and Table 1. Mtags are embedded in the data. Mtags represent the state of the cache as to the cache entry.

Regarding claim 16:

Kane teaches wherein the system comprises a plurality of processors, such that the system is a multi-processor system in paragraph 0002.

Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kane and ESC as applied to claim 10 above, and further in view of Zhang.

Regarding claim 12:

The teachings of Kane are outlined above.

Kane does not explicitly teach the cache being a multi-way cache. Kane does, however, teach an L2 cache and teaches that the teachings in the Kane reference can be applied to any type of storage or cache (see paragraph 0071).

Zhang teaches a multi-way cache in the entire document (see, for example, col. 2 lines 48-49).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the multi-way cache of Zhang with the caching system of Kane.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Kane teaches an L2 cache and teaches that the system and method can be applied to any type of storage device or cache. Zhang teaches that L2 caches are generally multi-way caches in col. 2 lines 34-36. Furthermore, multi-way caches provide greater speed, which meets Kane's stated need to meet performance expectations in paragraph 0004.

Regarding claim 17:

The teachings of Kane are outlined above.

Kane does not explicitly teach the system being a single processor system. Kane does, however, teach the teachings in the Kane reference can be applied to any type of system (see paragraphs 0071-0074).

Zhang teaches a single processor system in Fig. 1.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine single processor system of Zhang with the caching system of Kane.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Kane teaches that the system and method can be applied to any type of system or cache (see paragraphs 0071-0074). A single processor system, such as that of Zhang, is in widespread use in the art and is cheaper than a multi-processor system.

Allowable Subject Matter

Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests retrieving a second cache entry for the desired memory address and upon determining that the second ECC based at least on the second data of the second cache entry and the desired memory address equals the second stored ECC, concluding that the second cache entry caches the desired memory address without error as outlined in claim 5. All other allowable claims depend from claim 5 and include all limitations of claim 5.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Prior art cited by not relied upon by the examiner either contains elements of the instant invention or is provided to show the state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-T and TH-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

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